IMAPS-UK/NMI – Embedded Device Technology Conference

A Joint Event with

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Embedded Device Technology – burying silicon devices within circuit board materials – a process that would never work according to the experts in the 1990's, is coming of age in applications where size, cost and electrical performance are key to new product developments, according to Andreas Ostmann of Fraunhofer IZM, Germany, the keynote speaker at the jointly organised IMAPS-UK/NMI Conference, sponsored by Microsemi and held in the Mitel Facility in Caldicot, Wales.

This conference, attended by 58 people, covered a diverse range of topics, including the advances made in embedded device technologies, new application areas in solid state power modules and modular electronics and wearable devices, research into multi-physics modelling and prognostic system development and the current state of standard evolution.

The Keynote Presentation was by Dr Andreas Ostmann, Group Manager of Embedding & Substrate Technologies at the Fraunhofer Institute for Reliability and Microintegration, Berlin, Germany, who described the origins of the technology in 1968 in a patent filed by Philips, the developments through the 1990's, where there were many obstacles to overcome including accommodating the Coefficient of Thermal Expansion (CTE) mismatch between silicon and organic circuit board materials, through the industrial realisation phase in the 2000's, where several manufacturing options have been defined and to the present day, where several million devices are being produced per month in one application for production of DC/DC converters amongst others. For the future, modular electronics with common building blocks (e.g. temperature sensing, power management) each module with firmware/software will be designed and manufactured, the common blocks being used to assemble systems.

Nick Pearne from BPA Consulting proposed the idea of an "Organic Fab" concept for embedded device technology as a follow on from silicon fabs, incorporating active and passive components in large format working panels, creating a "One Stop Shop" for future electronics manufacture.

Steve Riches from Tribus-D described advances in techniques such as in-mould structural electronics and 3D printing that will create opportunities for embedding devices and presented some initial results from Imperial College on a laser based micro-joining process to produce robust joints on embedded device interconnections.

Stoyan Stoyanov from the University of Greenwich showed that multi-physics modelling techniques can assist in design optimisation through prediction of levels of warpage, lifetimes and material thickness optimisation, reducing the need for physical samples and testing, although not eliminating the physical prototype stages in product development.

Andrew Richardson from the University of Lancaster outlined an approach to implement "Biomorphic sensing" through self-monitoring, self-healing and self-adapting to achieve high levels of testability. They are interested in developing a "Self Validating Sensor Concept" with multi-

function sensors to provide cross functional sensitivities to assist in delivering systems with prognostic features.

At the end of the morning session, a hearty lunch was provided by the friendly and efficient servers from the Caldicot facility, when there was an active networking session whilst balancing the mountains of food.

After lunch, Cyril Buttsay from INSA, France demonstrated an approach for embedded power modules based on a DBC (Direct Bonded Copper on Ceramic) substrate, using die attach, PCB lamination and etching, laser ablation and electroplating techniques, all of which can be carried out on a low volume and prototyping basis, as well as for higher volume manufacturing.

Philip Ekkels from MbedICs-IMEC, Belgium presented a process to embed devices into a polyimide flexible circuit board substrate, using thinned die. The target markets include wearable devices such as connected patches and audiology devices and anti-tampering electronics. MbedICs – IMEC have US and European patents covering the process and are now looking for investors to take the process to market.

Chris Hunt from NPL indicated that there are several working groups within the International Standards community tackling the introduction of standards for embedded device technologies. IEC 62878 is the main working document for embedded device technologies and generic specifications are being developed to address various aspects of the subject. Inputs from interested parties to the Working Groups are welcome to assist in delivering standards.

Piers Tremlett from the Hosts and Sponsors - Microsemi described an embedded device assembly process to address lower volume applications to mobile phones to reduce size, minimise power and lower cost, using embedded die in printed circuit boards. This approach can realise several layers of embedded devices and a more rugged design with thicker copper tracks, but with lower track resolution than a fan out wafer level process, which can be used for low volume, high turnround, low non-recurring engineering (NRE) applications.

The presentations were rounded off by Kay Essig of ASE Europe, who informed the audience that ASE are manufacturing several embedded device products including DC/DC converters at volumes of 3.3M units/month with over 98% yield. The assembly process is called aEASI, where the route involves manufacturing components onto a leadframe, followed by lamination, etching, via ablation and electroplating. Design rules are available to enable users to design products to the manufacturing process.

The speakers were gathered for the post event photo-call and Patrick McNamee from NMI thanked the hosts, sponsors, speakers, organising committee and attendees for making the event work so successfully, in particular Rachel Palmer from NMI and Andy Longford from IMAPS-UK for their efforts in running the event.

For further information on the downloading the presentations, please contact Rachel Palmer, NMI or Andy Longford, IMAPS-UK.