SPW 2019

Semiconductor Packaging Workshop (SPW) – 6th June 2019

Electronics packaging and interconnection technologies determine the performance and efficiency of semiconductor devices and can account for up to 80% of the manufacturing costs. Knowledge of the materials and processing technologies involved in the assembly of electronic devices is key to optimising the performance, reliability and cost-effectiveness of electronics systems.

This IMAPS-UK organised Semiconductor Packaging Workshop provided a guide to help designers and engineers to navigate through the multitude of electronic packaging materials and processes. The workshop was hosted at Newport Wafer Fab, Newport, South Wales, was sponsored by Inseto and supported by the Compound Semiconductor Applications (CSA) Catapult.

This workshop was attended by 60 people to listen to and engage with leading proponents of electronics packaging. It covered a comprehensive range of topics, including: overview of package and substrate options, die preparation, attach and interconnection and quality assessment. The attendees had the opportunity to tour the wafer fabrication facilities at Newport Wafer Fab, participate in a packaging clinic and hear about the packaging capabilities being created at the Compound Semiconductor Applications Catapult Centre.

Package and Substrate Option

Andy Longford of Panda Europe described the status of electronic packages covering QFN, CSP, SiP, WLP, TSV, Flip chip and embedded device packaging. The profusion of different packaging options is challenging the established routes for manufacture; for example, wafer level packaging is generally carried out at the semiconductor foundry and embedded device packaging takes place at the circuit board level. The main driving forces for developing packaging technologies were to make components and modules smaller, faster and cheaper.

Steve Riches of Tribus-D presented an overview of the role of the electronic substrate to provide conductor paths, voltage isolation, heat dissipation, a base for mounting of components, connections and some mechanical and environmental protection. Although most applications use surface mount components assembled onto printed circuit boards, there is a myriad of other options available to the electronic designer. Future electronics applications will place additional demands on the substrate materials in order to achieve increasing levels of integration and miniaturisation at an affordable cost.

Die Preparation, Attach and Interconnection

Brian Raeburn of DISCO Europe described the main die preparation methods of dicing, grinding and polishing to meet the ever increasing demand for reduction in chip thickness. Details on DBG (Dicing Before

Grinding), Taiko Grinding, Blade Dicing, Laser Dicing and Stealth Laser Dicing processes were presented with advantages and limitations of each technique outlined.

Liam Mills of the Manufacturing Technology Centre (MTC) presented an overview of die attach and Interconnects processes which are two of the most critical processes for semiconductor packaging. The talk focused on Pb-free die attach options, their processes and associated failure modes, including a review of the latest sinter materials and Ag containing solder alloys. Interconnect technologies and their limitations were also described, including double sided solder bonding as an alternative for wirebonding to improve thermal performance and increase durability.

Quality Assessment

Sandeep Kullar of Nordson gave an overview of the test and inspection systems available from Nordson to inspect the smallest of features and detect a wide variety of different failure modes within semiconductor packaging. Wafer optical inspection, X-Ray (2D, 2.5D and 3D) and acoustic techniques and equipment were described, together with case studies of where the equipment has been used to identify failures and defects.

Compound Semiconductor Applications Catapult

Martin McHugh emphasised the growth opportunity for compound semiconductors and the role that the Compound Semiconductor Applications (CSA) Catapult will play in assisting in developing a UK based industry in this field. One of the priorities will be to drive forward the development of evaluation modules that will enable companies to assess their new applications and bring them to market faster in the three key application technologies of RF, Photonics and Power. An advanced packaging capability is critical to the realisation of products containing compound semiconductors. The approach to be taken will be to jointly develop the capability in collaboration with the current UK semiconductor packaging ecosystem and focus on value added unique processes within the CSA Catapult.

Packaging Clinic

An interactive packaging clinic was held to address the following questions:

- What are the current issues in electronics packaging?
- What are the major challenges to the introduction of new electronics packaging technologies?
- What can IMAPS-UK and the Catapult Centres do to support electronic packaging community?

The outputs from the clinic are being shared with the workshop attendees. One of key aspects discussed within the clinic were how to gain affordable access the Catapult capabilities within the UK, especially as it was perceived that there is some overlap between the Centres. Martin McHugh of CSA Catapult and Liam Mills of MTC described the activities being undertaken within the High Value Manufacturing Catapults to clarify their respective roles. Another important factor is knowledge sharing and brokerage within the packaging community and it was felt that IMAPS-UK could play a greater part in improving the networking activity.

The attendees also had the chance to network during the refreshment breaks. This workshop was very well received and another similar event will be planned in the future.

For further information, please visit IMAPS-UK (www.imaps.org.uk)