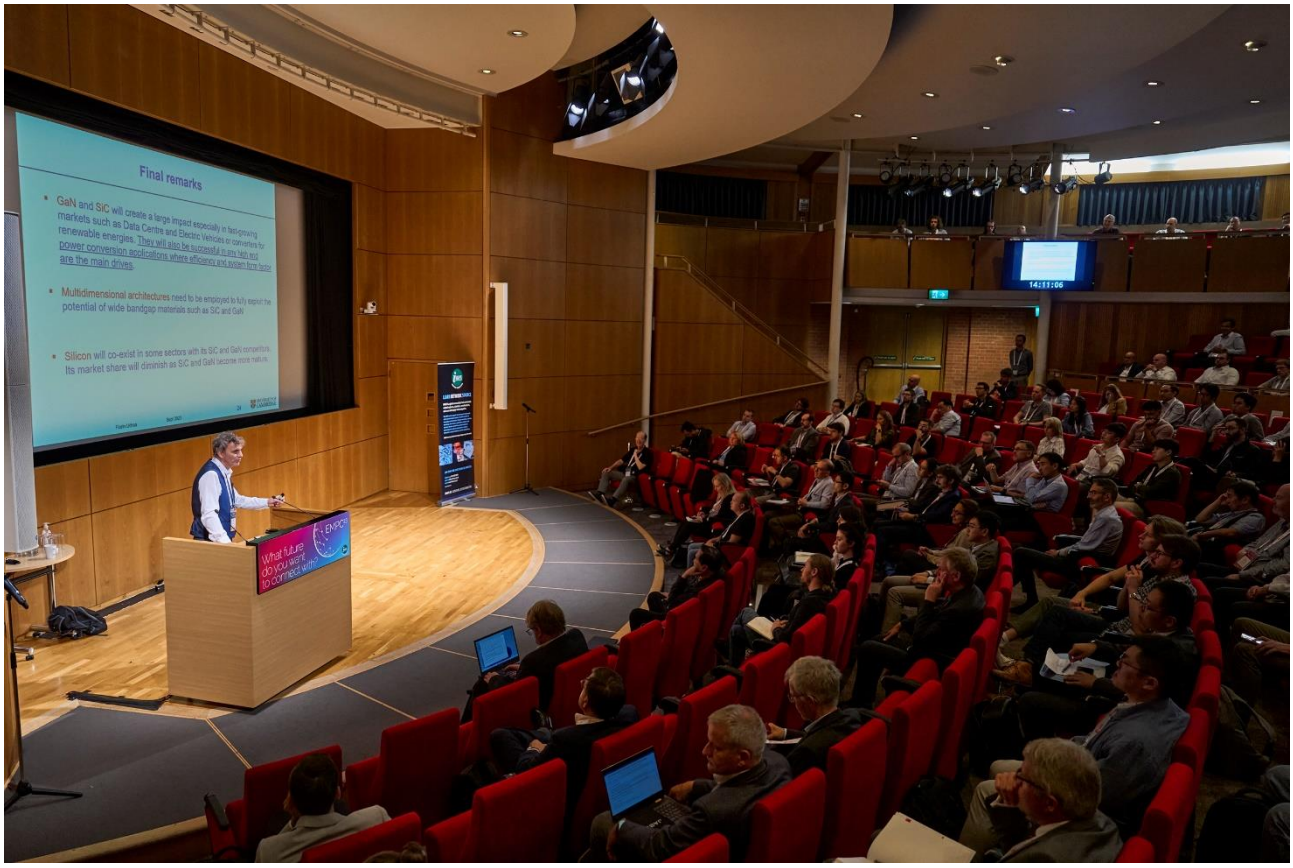
Conference Report on the European Microelectronics and Packaging Conference® 2023 (EMPC® 2023) held at the Wellcome Genome Campus, Hinxton, near Cambridge, UK

11 - 14 September 2023

IMAPS-UK hosted the European Microelectronics and Packaging Conference® 2023 (EMPC® 2023) in Cambridge, UK, with over 260 people attending over the three days of the in-person event. The Conference featured state of the art presentations from 5 keynote academic and industrial speakers, 70 oral and 18 poster presentations and 4 Professional Development Courses

The Conference Chair, Professor Anne Vanhoestenberghe (King's College London) welcomed participants to the event with an overview of IMAPS and of the activities over the three days of the Conference. The Conference Sponsors BESI, Accelonix, Inseto and Pactech and ASE Group and other exhibitors were thanked for their contribution to the Conference and the support of IEEE-EPS and IMAPS-Europe was acknowledged.



Day 1: Monday 11th September 2023

Professional Development Courses

- **Evolution of Die Attach Adhesives & Encapsulants Used in Semi-conductor Packaging** by Tony Winster, Henkel Ltd
- **Fan-out, Chiplet Design, and Heterogeneous Integration Packaging** by John H Lau, Unimicron Technology Corporation
- **Power Electronics Packaging – Understanding the Packaging Processes** by Andy Longford, PandA Europe
- **From Wafer to Panel Level Packaging** by Tanja Braun & Markus Wöhrmann, Fraunhofer IZM

40 people attended the courses throughout the day.

Day 2: Tuesday 12th September 2023

Keynote Presentation 1: Interconnecting Chiplets by Chris Scanlon, BESI Switzerland

The semiconductor industry is undergoing a shift from traditional transistor scaling to heterogeneous integration (HI) using chiplets. While System-on Chip (SoC) is becoming infeasible for some applications due to the limitations of Moore's Law, chiplets provide a way to continue system-level scaling through More than Moore. However, chiplet systems can be complex and require a hierarchy of different interconnect types in the same package. The most advanced interconnect technology for chiplets is hybrid bonding, which connects chips directly with Cu-Cu bonds. Die-to-wafer hybrid bonding has already been in volume production since 2022 for high-performance computing (HPC) applications. However, complete HI systems require other advanced wafer-level assembly processes as well, including TCB, fan-out and bridge die attach, wafer-level flip-chip, and wafer moulding. In the near future, photonic chiplets will be introduced, and together these interconnect methods can form a hierarchy of interconnect in complex chiplet systems. The different interconnect technologies used in chiplet systems and the advancements in assembly equipment that enable these high density interconnects were discussed. The importance of collaboration and standardisation in the chiplet ecosystem and how they can enable the rapid development of new products and business models were examined.

Session 1A: Substrates – LTCC and HTCC
Session Chair: Peter Barnwell, IMAPS-UK Trustee, UK

Contributions included High Frequency Bandwidth Transitions for HTCC packages from Egide in France, Reactive Bonding Methods for LTCC substrates from Saarland University in Germany and LTCC substrates for Trustworthy Electronics from VIA Electronic in Germany.

Session 1B: Embedding
Session Chair: Viorel Nicolau, "Dunarea de Jos" University of Galati, Romania

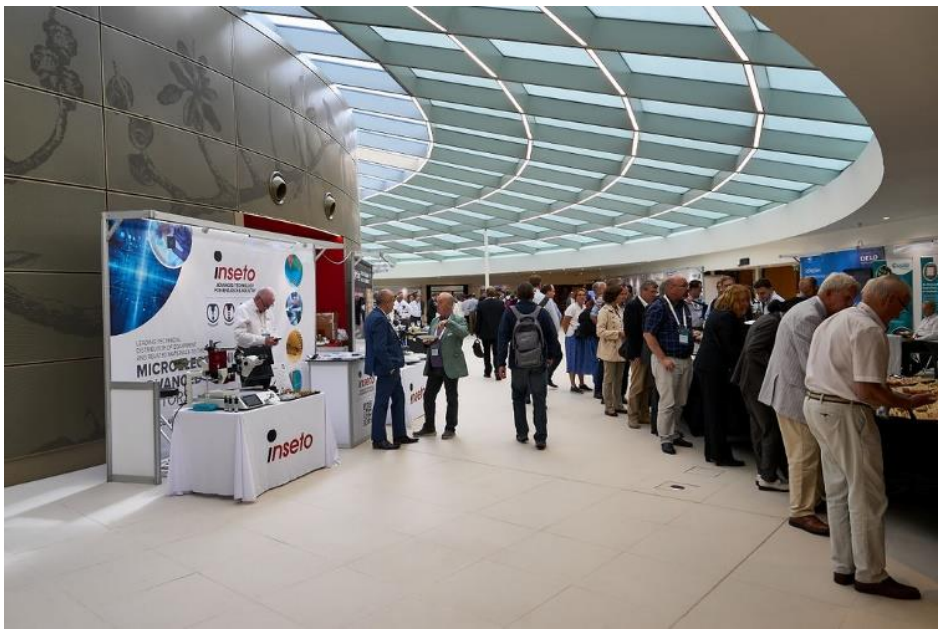
Presentations covered Embedding SiC Semiconductors for High Voltage Power Modules by Fraunhofer IZM in Germany, Ceramic Embedding of SiC Semiconductors using Co-Firing Technology by Fraunhofer IKTS in Germany and Characterisation of Embedded and Thinned RF chips by CETI in Germany

Session 2A: Interconnect Materials I
Session Chair: Rolf Aschenbrenner, Fraunhofer IZM, Germany

The four presentations were concerned with Deposition of Fine-Pitch Indium Bumps on Single Die by STFC-RAL in the UK, Silver Bonding Wire by Fraunhofer IMWS in Germany, Copper Pumping Analysis for Cu/SiO2 Hybrid Bonding by Silicon Austria Labs in Austria and Contact Resistance in ACF Bonding from Conpart in Norway.

Session 2B: MEMS/Sensors
Session Chair: Andrew Holland, RF Module And Optical Design Ltd., UK

Presentations were given on MEMS Mirrors in Hermetic Packages by ST Microelectronics in Italy, Silicon-Ceramic Technologies for High Strength Pressure Sensor Application by Technical University of Ilmenau in Germany, A Comprehensive Simulation Approach to Warpage for MEMS by ST Microelectronics in Italy and Protection Caps for Wafer Level Chip Scale Packaging for Environmental Sensors by Fraunhofer ISIT in Germany.



Keynote Presentation 2: Wide Bandgap Devices and Multi-dimensional Architectures in the New Era of Power Electronics by Professor Florin Udrea, Cambridge GaN Devices

The power devices field has seen tremendous changes in the last decade. Most of the innovation in the field comes from the emergence of Wide Bandgap semiconductors – and in particular those based on Gallium Nitride and Silicon Carbide. Extensive research is also carried out in single crystal Diamond, Gallium Oxide and Aluminium Nitride materials. The market of power devices has reached ~$50M with exponential growth in wide bandgap materials reaching CAGRs in excess of 50% in the next 3-5 years. This talk covered an extensive range of wide bandgap (WBG) and ultra wide bandgap (UWBG) semiconductor technologies and materials for power devices and addressed the new multi-dimensional architectures to further increase efficiency of power semiconductor devices.

Session 3A: Substrates – Thick Film and Cu Interconnects
Session Chair: Jens Müller, TU Ilmenau, Germany

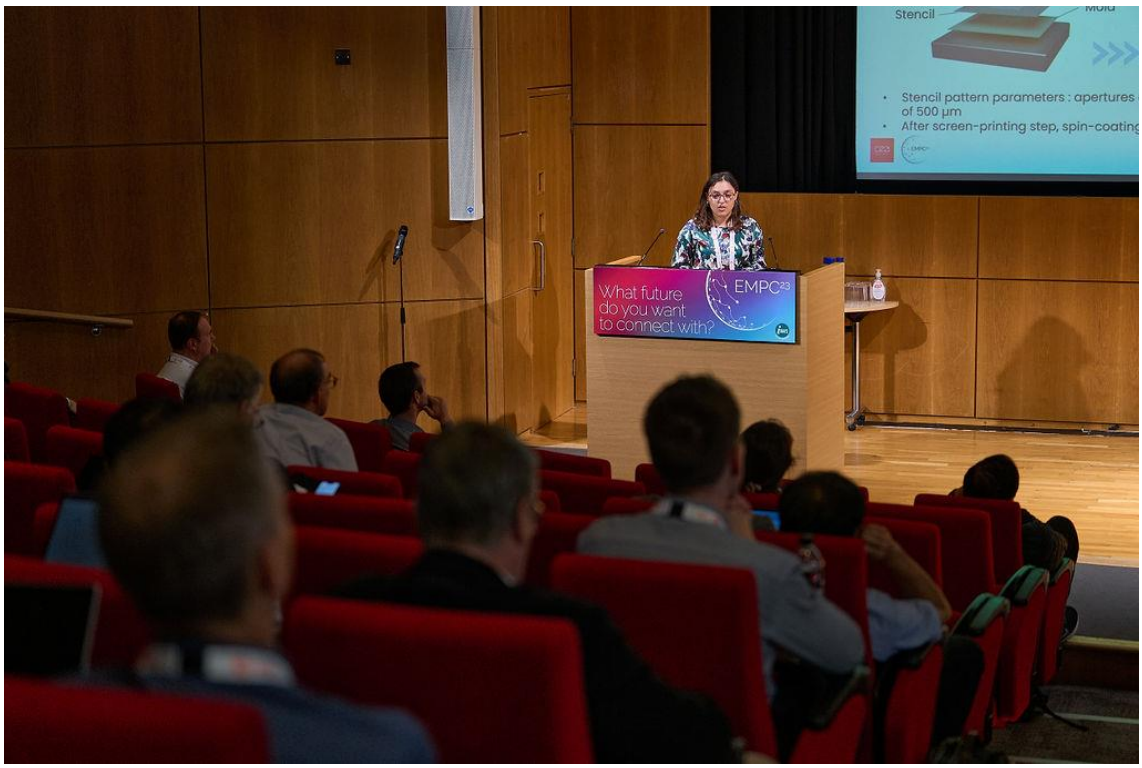
Contributions included Laser Fusion of Cu-Ti Powders for Metallisation of Alumina Substrates by the University of Erlangen-Nuremberg in Germany, Photo-Definable Polyimide with High Thermal Stability by Toray Industries in Japan and DIP based all Cu Interconnects by Dycotec Materials in the UK.

Session 3B: Adhesives and Encapsulants
Session Chair: Eamonn Redmond, Inseto (UK) Ltd, UK

Presentations covered Epoxy Moulding Compound Bleeding Reduction by ST Microelectronics in Italy, Influence of Thermally Aged Underfill on Flip-Chip Packages by Tektronix in the USA and Adhesive Solutions for Closed Cavity Packaging by DELO Industrie in Germany.

Session 4A: Interconnect Materials II
Session Chair: Olivér Krammer, BME, Hungary

The four presentations were concerned with the Development of Stretchable and Removable Electrical Interconnects for Ultra-Thin Components by CEA in France, UV Laser Copper Pad Surface Exposure for Laser Direct Structuring of Interconnects by ST Microelectronics in Italy, the Formation of Ag Nodules on Ag-Si Particles by Osaka University in Japan and Fine Pitch Micro Indium Bump Flip Chip Bonding by Finetech in Germany.

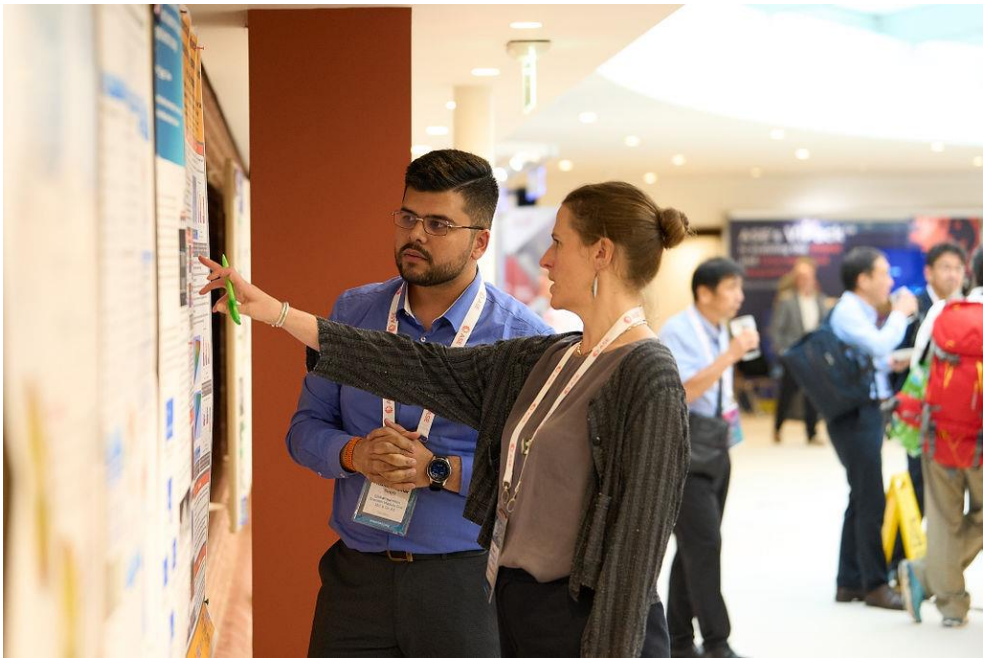


Session 4B: Medical
Session Chair: Anne Vanhoestenberghe, King's College London, UK

Presentations were given on Initial Life Tests of Silicone Encapsulated FR4 Printed Circuit Boards for Pre-Clinical Active Implants by University College London in the UK, Voiding in Parylene-C Encapsulation of Surface Mount LEDS for Epilepsy Neuroprosthesis by University College London in the UK, Printed Microfluidic Interconnects for Multiplexed SARS-COV-2 Receptor Binding Domain Protein Affinity Assays by the Hong Kong University of Science and Technology and Flexible Hybrid Electronics for Wearable Healthcare Application by ASE Group in Taiwan.

Poster Session

A poster session featured 18 posters with authors contributing from around the world.



Day 2: Wednesday 13th September 2023

Keynote Presentation 3: The Challenges of Integrating Graphene into Existing Packages by Ali Murad, Paragraf

Graphene has been one of the most exciting materials in recent years for a wide variety of industries ranging from electronics, energy, medicine, sensors, and many more. It has been referred to as a wonder material due to its incredible mechanical strength, lightness, flexibility, optical transparency, and impressive semiconductor properties (of both electricity and heat). Paragraf is the first company in the world to mass produce graphene-based electronic devices using standard semiconductor manufacturing processes and has been at the forefront of this effort. However, there are industrywide challenges related to graphene including, obtaining high-quality uniform contamination-free graphene, managing device integration to graphene and integrating graphene devices to industry standard packaging. This talk focused on how Paragraf is using its technology to solve real-world problems such as heat detection in EV batteries and brushless motors.

Session 5A: Sintering I
Session Chair: Martin Wickham, National Physical Laboratory, UK

Contributions included the Reliability of Copper Sintered Interconnects under Extreme Thermal Shock Conditions by the Technical Highschool Ingolstadt in Germany, Rapid Sintering of Inkjet Printed Cu Complex Inks by the Technical Highschool Ingolstadt in Germany and Improved Semiconductor Reliability of Silver Sinter Die Attach Materials for Large Die on Leadframe Applications by Henkel in the Netherlands.

Session 5B: Equipment/Inspection
Session Chair: Jeff Kettle, University of Glasgow, UK

Presentations covered Pick and Place of Sensitive Chips with Vacuum-Free Gecomer® Tools by Frainhofer IPMS in Germany, Research of Chip Placement Accuracy for Fan-Out WLP using a Novel Assembly Stage by LINTEC Corporation in Japan and One-Probe Nanoprobing o Power Devices and Electronic Packages by ZEISS Microscopy in the United States.

Session 6A: Photonics and Optics
Session Chair: Jayakrishnan Chandrappan, CSA Catapult, UK

Presentations were made on Spatial Distortion in InP Nanophotonics Membranes on Different Carrier Substrates by the Eindhoven University of Technology, The Netherlands, Laser-Assisted Bonding Approach for Photonic Integration Processes by Tampere University in Finland, Integration of Multi-Lithography Technologies for the Fabrication of Flexible Optical Link by the Technical University of Dresden in Germany and Hybrid Lithography Fabrication of Single Mode Optics for Signal Redistribution and Coupling by the Technical University of Dresden in Germany.

Session 6B: Solders/Soldering
Session Chair: Attila Géczy, BME University, Hungary

The presentations covered Comparing the Solderability of Different SAC307 Composite Solder Pastes by the Budapest University of Technology and Economics in Hungary, Anisotropic Solder Paste Material for Laser Assisted Bonding Process by ETRI in South Korea and Durability Distribution Analysis of Lead-Free Solder Interconnections for Printed Circuit Applications by the University of Maryland in the United States.

Keynote Presentation 4: Advanced Packaging - Challenges that are driving new package innovation and ecosystem needs by Mark Gerber, ASE Group

Advanced silicon node challenges, and the drive within industry to find new ways of offering the highest level of performance, are driving many new ways to extend advanced packaging. Many analysts defined advanced packaging as packaging that uses a higher density of interconnect, outside of the traditional wire-bond. This category opens a broad spectrum of packaging solutions that include, Flip Chip, Fan Out Wafer Level Packaging, Hybrid Packaging, System in Package, 2.5D/3D and many other sub-categories. As yield enhancement and performance improvements are driving design considerations, such as heterogeneous and homogenous integration, it is becoming more complex to navigate this plethora of new options and to understand the key trade-offs in selecting the right package solution. Challenges including power delivery signal integrity, multi-physics impacts, IP block interface standards, chiplet manufacturing considerations, warpage and many others are driving the ecosystem to change to meet these new and evolving needs. The traditional 2D mindset for silicon integration in packaging is rapidly changing and a 3D or vertical mindset is becoming a key driver for HPC, AI and is extending into mobile products.

Session 7A: Sintering II
Session Chair: Andy Longford, PandA Europe; UK

Contributions included an Investigation of the Mechanical and Thermal Properties of a Silver Oxalate Sintered Joint by VALEO in France, Understanding the Effect of Porosity of Corrosion Behaviour of Cu Sintered Paste for High Temperature Microelectronic Application by Liverpool John Moores University in the UK and Inspection Techniques using Scanning Acoustic Microscopy for Silver Sintering Applications in Power Electronic Modules by the University of Warwick in the UK.

Session 7B: Hermetic/Conformal Coating/Thermal Interface Materials
Session Chair: Hassan Akhtar, Manufacturing Technology Centre, UK

The presentations covered Characterisation of a Novel Graphene-Enhanced Thermal Interface Material by Shanghai University in China, Evolution of Getter Technology in Electronic Hermetic Packaging by SAES Getters in Italy and Advanced in Parylene Adhesive Bonding for the Realisation o Biocompatible Microsystems by Fraunhofer ENAS in Germany.

Session 8A: Flip Chip
Session Chair: John Lipp, STFC, UK

Four presentations were made on Flip-Chip Interconnects based on Single Metal Coated Polymer Spheres by the University of South-Eastern Norway, 20 micron Copper Micro-Bump Bonding through a Silver Metallisation for Advanced Packaging by Osaka University in Japan, Practical Results of Demonstrate an Increase in Reliability of Flip-Chip Connections by Adding Nano-Particles to Solder by Liverpool John Morres University in the UK and Development and Characterisations of Fine-Pitch Flip-Chip Interconnections using Silver Sintering by CEA LETI in France.

Session 8B: Reliability and Sustainability
Session Chair: Derek Braden, Aptiv, UK

Presentations were given on an Analysis of the Impact of Environmental Conditions on the Reliability in 5G PCB assemblies by Fraunhofer IZM in Germany, Evaluation of the Environmental Impact of Solders and IC Packaging Techniques by the University of Glasgow in the UK, Combined Measurement of Temperature and Straining of a PCB during Operation using Stereo DIC and Thermal Camera by MatchID in Belgium and Measurement and Simulation of Mechanical Strength of Back-End-of-Line Layer in Advanced CMOS Die by IMEC in Belgium.

Networking Dinner at Homerton College

Day 3: Thursday 14th September 2023

Keynote Presentation 5: Reinventing Electronics for a Sustainable World by Feras Alkhalil, Pragmatic Semiconductor

Tackling challenges associated with the climate crisis, sustainability of food supplies and healthcare inequalities require innovative sustainable approaches. Pragmatic Semiconductor is a world leader in the design, development and manufacture of ultra-lowcost Flexible Integrated Circuits (FlexICs). Pragmatic's FlexICs technology is unique in allowing designers to access extremely agile design cycles, coupled with a low cost and low environmental footprint distributed manufacturing model, this enables sustainable democratised innovation. Pragmatic's innovative FlexIC Foundry™, offering novel form-factor integrated circuits, that can be used to create ubiquitous low-cost smart systems was presented, along with details of novel emerging technologies, that are currently being developed, that will enable designers to create even more innovative designs.

Session 9A: Machine Learning
Session Chair: Stephen Riches, IMAPS-UK, UK

Contributions included Application of Machine Learning Methods for Process Optimisation in Electronic Packaging Processes by Robrt Bosch in Germany, Using Deep Learning Reconstruction for High Throughput and High Resolution 3D Analysis of Packaged Wafers by Carl Zeiss in the UK and Partial Discharge Characterisation of Ceramic Power Electronics Circuit Carriers assisted by Machine Learning by Fraunhofer IKTS in Germany.

Session 9B: Solar/Sensors
Session Chair: Knut E Aasmundtveit, University of South-Eastern Norway, Norway

The presentations covered Impact of Pad Layouts and Solder Volume on Self-Alignment of Micro Solar Cells by Fraunhofer ISE in Germany and Novel Low Temperature of Low Pressure Sintering of ADAS Radar Sensor Attenna Stack by Technical Highschool Ingolstadt in Germany.

Session 10A: High Frequency
Session Chair: Ivan Ndip, Fraunhofer IZM and BTU Cottbus-Senftenberg, Germany

Four presentations were made on Characterisation for EWLB Antenna in Moulded Package Integrations in 77Ghz Automotive Applications by JCET Group in Singapore, A Dual-Band, Dual Polarised 2x2 Antenna Array with Beamforming for 5G AIP and mmWave Applications by ASE Group in Taiwan, Analysis and Characterisation of Castellated Holes as RF Interconnects for Modular mmWave Devices by Technical University Berlin in Germany and High Q KU Band Microstrip Spiral Resonator in Fan-Out Wafer Level Packaging for VCO Applications by Fraunhofer IZM in Germany.

Session 10B: Power Modules
Session Chair: Andy Longford, PandA Europe, UK

The five presentations covered Bacchus – An Adaptable Format Power Module for Low Volume Designs by Microchip in the UK, Thermal-Mechanical Analysis of a Power Module with Parametric Model Order Reduction by the University of Greenwich in the UK, Thickness Effect of Copper Clips on Power Module Packaging Design by the University of Warwick in the UK, High Frequency Thin-Film Magnetics-on-Silicon with Improved Inductance and Resistance by Wurth Electronics in Germany and Enhanced Reliability for Power Modules via a New Ag/Si Sinter Joining Strategy by Osaka University in Japan.

Awards for Oral Presentations

- Best Paper – Development and Characterisation of Fine Pitch Flip-Chip Interconnection using Silver Sintering by Julle Gougeon of CEA-LETI in France
- Highly Commended – Development of a Stretchable and Removable Electrical Interconnect Solution for Ultra-Thin Electronic Components by Auriane Despax-Ferreres of CEA-LITEN in France

Awards for Poster Presentations

- Best Poster – Improved of Bonding Strength and Thermal Shock Reliability for Ag Sinter Joining Direct on Al Substrate by Chuantong Chen of Osaka University in Japan
- Highly Commended – Reliability Testing of Recycled SMD Components Re-used in E-Textiles after Ageing by Washing Cycles by Martin Hirman of University of West Bohemia, Czech Republic

Closing Session

Professor Anne Vanhoestenberghe thanked attendees at the Conference, for the support from the IMAPS-Europe and IEEE-EPS, the organising team at MCC-Events (Martina Creutzfeldt, Ajda Omrani and Rahel Dietze) and at IMAPS-UK (Martin Wickham, John Lipp, Eamonn Redmond, Andrew Holland, Scott Wood and Steve Riches) in putting the Conference together over the past two years. The support of the Exhibitors and Sponsors was also acknowledged, along with the contributions from the Session Chairs and Technical Committee in reviewing and selecting the papers and posters.

Jean-Mark Yannou (ASE Group) announced that the EMPC® 2025 Conference will be held in Grenoble, France in September 2025. Further details about the Conference will be provided in due course.