IPower5 Conference – Get Up to Speed

Wednesday 29th November 2023 – Held at the British Motor Museum, Gaydon, Warwickshire

The IMAPS-UK organised iPower5 Conference and Exhibition took place on Wednesday 29th November 2023 focused on state of art presentations on power electronics packaging including sessions on advances in devices and modules, sintering, dicing, trimming and forming. A discussion session on the UK National Semiconductor Infrastructure Strategy on Advanced Packaging was also held.

The Conference Chair, Martin Wickham (NPL and IMAPS-UK Vice-Chair) welcomed participants to the event with an introduction to IMAPS-UK.

The Conference Sponsor, **Carl Zeiss Ltd,** represented by Andrew Elliott gave an overview of their capabilities covering several microscopy solutions used for nano and micro applications.

Session 1: Devices and Modules

Keynote Presentation:
Latest Advances in Devices and Modules for Electric Vehicles – Phil Mawby, University of Warwick

The uptake of electric vehicles was outlined in this presentation, where fleet vehicles are seeing significant growth, amongst the 20% of new vehicles registered that are electric. The UK has a limited capability for the manufacture of semiconductor devices, although there are still some foundry facilities which can produce wide band gap devices required.

The need to establish supply chains for the manufacture of power electronics modules was explained and two major projects (ESCAPE and FutureBEV) partially funded by Innovate UK through the Advanced Propulsion Centre (APC) were described. These projects are coming to an end, where supply chains have been created to be exploited in the UK in the future.

Embedded PCB Power Modules – Stylianos Syrigos, Microchip Technology Inc

Embedded die power modules appear to be a new trend in power electronics packaging, offering benefits such as custom module geometry, miniaturization, low parasitics and reduced packaging cost. This presentation focused on low (Switched Mode Power Supply - SMPS)) and medium power (Motor Drive) embedded die applications (up to 10kW) for the aerospace sector. Starting from the concept inception, each step of the design process was thoroughly analysed, including layout, electrical and thermal FEM simulations. Special attention is given to the thermal extraction mechanism, which is key for any demanding power electronics application. Finally, the build process steps were described, starting from a simple PCB panel to a finished embedded die PCB power module, giving emphasis to the low-cost character of the build process, which can be realised through build on large area panels.

Modelling the Impact of Cosmic Rays on the Reliability of Power Semiconductor Devices – Gabriel Parkinson, University of Nottingham

The presentation covered Cosmic rays (primary and secondary), the cosmic ray energy spectrum in near-Earth orbit and within the Earth's atmosphere, the composition of secondary cosmic ray particle cascades, why it is important to consider cosmic rays when designing power semiconductor devices, the state-of-the-art in power devices radiation hardness testing and in modelling heavy ion and secondary cosmic ray interactions with power semiconductor devices. The implications of this study could have an impact on the reliability of devices operating in aerospace and other extreme environments and the device design may need to be optimised to avoid high electric field densities and thinned materials. The question of whether GaN devices are less susceptible to these effects was raised.

Session 2: Sintering

(Hybrid) Sintering Materials for High Power, High Temperature Applications – Jochen Schuermans, Roartis – presented remotely

Over the past years, power electronics have become more mainstream in various applications, such as electric vehicles, telecommunications, defence, aerospace, and aviation applications. Where traditional die-attach adhesives were limited in high thermal conductivity features, and soldering solutions were still the primary choice for thermal dissipation, sintering materials have been able to fill that gap for certain applications. However, despite the great interest in sintering materials, they also are limited for certain applications where CTE mismatch are a concern.

To overcome certain of those limitations, a new set of hybrid sintering materials has been developed, based on “green”, environmental friendly chemistry. The presentation described these new hybrid sintering materials and provided a detailed introduction on major parameters, such as particle size, shape and composition, additives, sintering parameters and metallisations that have an influence on overall sintering performance.

Novel Interconnect and Packaging Technologies for Power Modules – Huub Claassen, Boschman Technologies

For these high-power applications, the conventional semiconductor material – Silicon (Si) – is reaching its physical limits it terms of power density, switching frequency, operating temperature, and breakdown voltage. As a result, the industry is moving to next generation semiconductor materials, so called Wide-bandgap materials (WBG) to replace Silicon (Si) such as Silicon Carbide (SiC) and Gallium Nitride (GaN).

While these materials offer breakthrough properties, they are not a drop-in replacement and essentially require all new designs, materials, and processes to deal with higher temperatures and offer better thermal resistance, performance and reliability. Specifically, for back-end semiconductor packaging:

- Silver Sintering (to replace and overcome thermal limitations of tin-based solders)
- Epoxy Moulding (to replace and overcome thermal limitations of silicone gel)

Boschman has pioneered both processes with early adopters in the industry for both Pressure Sintering and Advanced Transfer Moulding. For Pressure Sintering, developments are expanding beyond die attach to include top side assembly, package to heatsink manufacture and wafer lamination sintering. For Advanced Transfer Moulding, attention is focused on film assisted moulding and dynamic inserts to apply specific levels of pressure to different devices within the power module.

Scanning Acoustic Microscopy of Sintered Joints – Heaklig Ayala, University of Warwick

Today, the necessity of rapid development and prototyping of power electronic packages demands a pragmatic approach to Scanning Acoustic Microscopy (SAM). The technology holds significant potential in Ag-sintering applications for power electronic modules and devices. Nevertheless, it often remains little understood to many who could benefit from its numerous advantages. This presentation aims explained the typical challenges and limitations to consider when performing C-SAM for the inspection and analysis of microstructures within power electronic devices, placing a particular focus on silver-sintered interconnects. The presentation included several acoustic images, including discrete devices in TO-247 packages, power modules, and custom samples of substrates and devices. Typical defects, including voids, cracks, and delamination, were identified. The presentation also delved into hurdles associated with surface finishes interfering with the inspection of Ag-sintered layers and demonstrated the distinguishing levels of warpage within power modules.

Session 3: UK National Semiconductor Infrastructure Strategy

UK National Semiconductor Strategy – Charles Sturman, Techworks

This presentation by Charles Sturman of Techworks (standing in for John Lincoln of the Photonics Leadership Group) reported on the preliminary outcomes of the Semiconductor Infrastructure Feasibility Study organised by the Institute for Manufacturing (IfM) – Engage team as part of a DSIT Semiconductor Strategy Review in collaboration with several other partners including: CSA Catapult, Techworks, Silicon Catapult, Photonics Leadership Group, Semiwise, Future Horizons, Cambridge Econometrics, Imperial College and the University of Leeds.

The initial outputs of the study were presented covering the following 5 main areas:

- Silicon Manufacturing (WP1)
- Advanced Packaging (WP2)
- Compound Semiconductor Open Access Foundry (WP3)
- Design IP/Tooling Capabilities (WP4)
- Strategic Co-ordination (WP5)

The report produced by the IFM-Engage team will be submitted to DSIT in the coming month and is likely to be considered in the next UK Government Spending review in scheduled for later in 2024. Implementation of the proposed plan should depend on the outcome of this review.

UK National Semiconductor Strategy on Advanced Packaging Discussion facilitated by Andy Longford, PandA Europe

This discussion focused on the Advanced Packaging topic, where several initiatives have been instigated in other countries, including the USA, Europe and Japan. In the UK, an Advanced Packaging Facility has been proposed to create Research and Development capabilities for Heterogeneous Integration as a potential outcome of the feasibility study.

Inputs were requested from the iPower5 Conference delegates, where the following points were noted:

- Any capability created should also have the remit to carry out prototype or limited production to ensure R&D can be converted into reality using state-of-the-art equipment
- Attracting global foundries to the UK will require many Billions and may face challenges with providing subsidies to overseas companies
- The power electronics sector is under-represented in the Semiconductor Strategy, where there is potential for growth within the UK manufacturing infrastructure. Some activities in WP3 for Compound Semiconductors Open Access have been identified
- Currently the largest semiconductor foundry in the UK has a power device capability
- Semiconductor fabrication has some traction in the UK Government under the auspices of Net Zero and Levelling Up
- Is there a requirement for Heterogeneous Integration along the lines being developed for consumer mobile communications (e.g. Apple, Samsung)?
- Should funds be concentrated on developing existing local cluster capabilities rather than a new central facility?
- Mixing of technologies (e.g. photonics and digital) could be a future route for the next generation of electronics, which will require Heterogeneous Integration
- There is not enough money in the budget to do everything proposed.
- On a show of hands by the delegates there was mixed support for the creation of the HI R&D facility.

Further comments on the Semiconductor Infrastructure are welcome and can be routed through the IMAPS-UK Office (office@imaps.org.uk).

Session 4: Dicing and Trimming/Forming

Plasma Dicing of SiC Semiconductors – Richard Barnett, KLA Corporation

According to a recent Yole report, dicing yield for SiC devices is around 91%. Whilst there are more pressing concerns at the substrate level, as SiC production matures and grows, yield gains will be sought from across the process flow. Plasma dicing of Si is being adopted to take advantage of the benefits afforded by using plasma versus the more traditional mechanical techniques. This is allowing manufacturers to alter their wafer layouts to increase the die per wafer count, generate stronger and cleaner die. This presentation introduced the plasma dicing concept, highlighting the potential gains that could be achieved in silicon device manufacturing and looked at the potential rewards from applying the techniques to SiC devices, including reduced cut widths, less chipping and cracking, which results in enhanced die reliability. Integrating the plasma dicing process within an overall manufacturing flow and dealing with backside metallisation on power devices remains a challenge to be overcome.

A Correlative Study between Shear Testing of X-Ray CT as Analytical Tools for Ultrasonic Weld Quality – Steven Derksen, TFA Trim and Form

Silicon-Carbide (SiC) devices with superior performance over traditional silicon power devices have become the prime candidates for future high-performance power electronics energy conversion. This presentation provided a review of the state-of-art advanced module packaging technologies for SiC devices with the focus on moulded power modules, the final assembly steps such as the Trim and Form process, and adding

Laser marking / deflashing / AOI functionality to create the perfect Signal pins and Power connections, instead of the traditional injection moulded case based glob top vertical pin contact style IGBT's.

To fully exploit the advances in manufacturing SiC devices, the packaging solutions focused on exploiting the benefits of Automation, where several options were described for dambar cutting, gate remain removal and final leadlength cut.

Meet the Exhibitors

The following organisations exhibited at the iPower4 Conference:

Accelonix - Specialist Equipment Sales and support for Microelectronics, Battery and PCB Assembly

Carl Zeiss— Materials Characterisation and Failure Analysis

DISCO Hi-TEC Europe GmbH – Semiconductor Dicing and Grinding Solutions

Inseto (UK) Ltd—Manufacturing Equipment, Assembly Materials and Adhesives

PPM Power – Power Electronics, Power Supplies, Test and Systems

Rydon Technology – Specialists in the supply of quality precision equipment and materials for high technology industries

Tresky – Leading Machine Manufacturer of High Precision Placement Systems

For further information on forthcoming events, please visit IMAPS-UK (www.imaps.org.uk)