MicroTech 2026 Conference – Driving Innovation in Semiconductor Packaging

Thursday 26th March 2026 – Held at the King's Conference Centre, Hedge End, Southampton

The IMAPS-UK organised MicroTech 2026 Conference on Driving Innovation in Semiconductor Packaging explored the themes of advanced packaging and heterogeneous integration, with 104 delegates attending.

This MicroTech 2026 Conference Report covers the following areas:

- Conference Presentations
- Meet the Sponsors and Exhibitors
- Poster Presentations
- Heterogeneous Integration – Explained! Workshop

MicroTech 2026 Conference Presentations

The MIcroTech 2026 Conference Chair, Eamonn Redmond, welcomed participants to the event with an introduction to IMAPS-UK.

Session 1: Semiconductor Packaging – Market and UK Strategy

Keynote Presentation – Introduction to the UK Semiconductor Centre by Mike Bishop, UK Semiconductor Centre

The UK Semiconductor Centre (UKSC) is a strategic hub, set up in 2025, to connect, unite and promote the industry in the UK. Its goal is to realise the full potential of the UK semiconductor industry by maximising opportunities, growth and reach. This presentation provided an introductory overview of the UKSC, explaining its five core missions and some of the early activities in which it is engaging. The presentation also summarised findings from the UKSC's roadshow that took place at the end of last year, engaging with over 400 members of the semiconductor industry across the UK. Finally, the presentation outlined how delegates can find out more and get involved with the UKSC's missions

Keynote Presentation - Advanced Packaging Technology and Manufacturing Trends by John West, Yole Group

The semiconductor industry is undergoing multi-front disruption, driven by technology, manufacturing complexity, and shifting end-market demands. AI workloads are the primary growth engine, accelerating demand for GPUs and AI-specific ASICs in data centres for large-scale training and inference. High-performance packaging is now a critical enabler, as advanced AI processors face increasing power, bandwidth, and thermal constraints. 2.5D interposers and 3D stacking have emerged as the dominant interconnect technologies for AI processors, enabling higher integration density and improved system performance. Autonomous and edge applications, particularly vehicles, are driving demand for low-latency, high-performance compute platforms with increased sensor integration. Next-generation packaging platforms —including panel-level packaging (PLP), CoPoS, CoWoP, and glass core substrates—are under active development to support future scalability, performance, and cost efficiency for AI systems.

Session 2: Advanced Packaging

Laser Solder Jetting and Laser Assisted Bonding and Reflow by Thomas Oppert, PacTech

The miniaturisation in electronics is driven by size reduction and cost, whilst increasing the technical performance of the device. Technologies with the potential of highest integration and cost savings are needed. Wire-bonding is still the most common bonding technology for creating electrical interconnects as well as flip chip technology for interconnects where the standard wire-bonding processes reach the limit. For these technologies and advanced packaging in general, new processes have been developed.

In part one of the presentation a laser soldering process was introduced. This process is a technique that drops a preformed solder sphere onto the bond pad while simultaneously reflowing the ball in-place using a laser. This tool has been used for many years in the industry; it is commonly known in the industry as a solder ball bumping tool. and the process has been scaled down for processing solder spheres with a diameter down to 30µm.

After pre-soldering, the devices need an assembly method to connect the chip to the substrate. In part two of the presentation, such an assembly process was described. For assembling a chip to a substrate, a laser assisted chip bonding technology (LAB) and laser assisted reflow (LAR) has been developed. The process principle of both, LAB and LAR and its benefits as well as the motivation were explained.

The presentation was completed by Adam Short who demonstrated the laser soldering process at recently installed equipment at Custom Interconnect Ltd.

Fluxless Die-to-Wafer TCB: A Reliable and Contamination Free Approach to 3D Integration by Jonathan Abdilla, BESI

Die-to-wafer (D2W) thermo-compression bonding (TCB) is a key enabling technology for 3D integrated circuits, but traditional bonding processes often rely on fluxes to facilitate solder based bonding, which can lead to contamination, reduced yields, and decreased reliability. Fluxless TCB, on the other hand, offers a promising alternative, eliminating the need for fluxes and enabling a cleaner, more reliable bonding process. This presentation gave an overview of the market current and future needs, where TCB fits and

also discussed the latest advancements in fluxless D2W TCB. The key criteria for a fluxless D2W TC bonder were highlighted so as to better understand the difference compared to traditional TC bonders. Typical process flows for fluxless TCB were reviewed and provided a comparison of different methods of fluxless bonding in the field. Results demonstrating the reduction of oxide levels, cross sections of bonds done at 10µm pitch and below as well as for Cu-Cu solderless bonding were shown. Electrical test results also demonstrated the link between bond quality with yield.

Session 3: Heterogeneous Integration

Keynote Presentation: CHIMES: Making UK Electronic System Design Globally Competitive by John Darlington, University of Southampton

Electronic product design has benefitted from key industry drivers; semiconductors ability to shrink transistors and hence functionality into ever smaller geometries; IP licensing enabling more functions in single System on Chip die, standardised die packaging supporting global component supply and regularised PCB manufacturing.

Globally leading companies are changing the approach to design and manufacture of electronic systems via Heterogeneous Integration. The UK electronics sector stands at a crossroads, stick to what we know or embrace recent advances to develop world leading products.

As part of the UK investment in semiconductors, CHIMES is one of four Innovation and Knowledge Centres, with a focus on Heterogeneous Integration of MicroElectronic and Semiconductor Systems. The centre aims to mimic the unique attributes of HI, bringing together UK capabilities in; Research and Development; Systems Design, Manufacturing and associated activities to help the UK adopt these latest advances.

The IKC was presented and it's aims and work plans were described to help industry to transition current electronic-based systems design to adopt HI to remain competitive in global markets.

The Development of a UK Based Supply Chain for Silicon and Glass Based Packaging Platform for Advanced Packaging Applications by Ben Nicholson, BAE Systems

This talk outlined the ongoing development of a UK supply chain for silicon and glass interposers targeting the niche and low volume electronics markets. The initial Innovate UK project, InterposeUK (2025), successfully demonstrated the fabrication of silicon and glass interposers featuring 40µm copper filled vias and redistribution layers with single digit micron track and gap widths, representing a significant step beyond current PCB capabilities. Such interposer technology is essential to the global shift towards Advanced Packaging and Heterogeneous Integration.

Building on this foundation, the follow up project, CHIPSET, is now nearing completion. Its focus is on enhancing interposer performance by maturing the flip chip bonding processes and developing a more advanced redistribution layer through the inclusion of integrated passive components. Embedding passive components within the interposer itself, rather than requiring soldered surface mount components, offers some key benefits; reduced size and weight, and improved electrical performance through minimising parasitics from shorter interconnect lengths.

This talk explored global trends driving the need for interposers and advanced packaging. It then highlighted recent progress in the fabrication of silicon and glass interposers, including how they impact current PCB designs. Finally, it considered the future direction of Advanced Packaging and Heterogeneous Integration.

A Customisable Interposer Based Packaging Platform for Heterogeneous Integration by Chris Lewins, Hybrid Integration

New and emerging chip technologies demand high-speed, high-density and photonic connectivity to realise their full potential. Advanced packaging is key to bringing electronic and photonic chiplets together, but these solutions are largely confined to high-volume consumer products from large semiconductor companies. For innovators developing low-to-medium-volume systems, suitable advanced packaging is effectively out of reachwhere they must rely on legacy approaches that sacrifice performance or invest in costly bespoke solutions. This highlights the need for a flexible, cost-effective platform that enables hybrid integration and high-performance interconnects.

Early details of a rapid-turnaround, customisable packaging platform that addresses this gap were presented. The platform is designed to enable flip-chip, area-array connectivity to minimise RF parasitics and maximise interconnect density. The interposer and assembly fabrication capability were described and preliminary interconnect performance data for the platform were provided. To do this, several types of prototype die and interposer containing test structures have been fabricated, which have been assembled using a flip-chip process. Dedicated RF test structures to characterise the high-frequency performance of the interconnected die and interposer have been developed, which were benchmarked against traditional wirebonding approaches. Daisy-chain structures to characterise the low frequency and mechanical performance of the interconnect between interposer and die were used.

How this platform could accelerate development cycles, reduce cost and lead time was discussed, offering a commercially and technically feasible approach for innovators seeking advanced hybrid integration.

Session 4: Applications

Top-Side Cooling Integration in Power MOSFET Packaging for Automotive and High-Performance Application by Dolores Milo and Christopher Liu, Nexperia

This presentation investigated Top-Side Cooling (TSC) as advanced thermal management strategy for silicon-based power MOSFET discrete packages, addressing the growing challenge of increasing power density in modern electronic systems. Applications such as automotive power modules demand compact designs, high performance, and long-term reliability, but traditional bottom-side cooling (BSC) methods are limited by PCB thermal properties and restricted heat conduction paths. These constraints hinder effective junction temperature control and reduce overall system efficiency.

The study conducted a comparative analysis of TSC and BSC, focusing on key thermal metrics including junction temperature (Tj) and thermal resistance (Rth). It examined how TSC improves heat extraction by enabling more direct heat transfer from the device surface to external cooling structures. Critical design factors—such as the selection and optimization of thermal interface materials, heatsink attachment methods, and package-level adaptations—were evaluated to understand their impact on thermal performance.

Through simulation and experimental validation, the results demonstrated that TSC significantly lowers thermal resistance, enhances heat spreading, and supports higher current capability. Automotive-grade case studies further confirmed its advantages under demanding operating conditions. Overall, the presentation concluded that TSC is a highly effective, scalable alternative to conventional cooling, offering improved thermal efficiency, power density, and system reliability.

Novel Technique for Scanning a 4 x 5mm Semiconductor Chip comprising multiple 12 x12 QLE Matrices and Mapping the sub-micron XY Co-ordinates of the QLEs and their Mode Centres by Phil Mitchell, Bay Photonics

As quantum applications continue to grow, the semiconductor devices required to support these new applications also evolve. Microelectronic packaging processes must also evolve to provide a suitable operating environment for these quantum semiconductor devices.

Currently aligning optical fibres to semiconductor devices such as lasers and photodiodes requires either the laser to be emitting and the fiber aligned for maximum coupling efficiency, or for a photodiode, an active fiber alignment process targeting maximum photodiode photocurrent.

However, for non-lasing devices like quantum light emitters (QLEs) which only emit single photons whilst operating at cryogenic temperatures, other practical non-emitting methods of fibre alignment must be developed which can be reliability performed at room temperature.

Bay Photonics in collaboration with the IUK SPARQLE project partners have developed a method of Optical Coherence Tomography (OCT) which can be used to scan a 4x5mm semiconductor chip comprising multiple 12x12 QLE matrices and mapping the sub-micron XY coordinates of the individual QLEs including their resonant mode centres. The spectral absorption properties of the semiconductor materials can be used to develop an image in sub-micron resolution of the QLE structure itself, providing an image of the QLE's outer trench structures, its circular photonic crystal resonator or circular Bragg grating (CBG), its central disk bullseye, and other chip growth anomalies. Finally a sub-micron resolution sweep around the QLE bullseye central disk provides detection of the QLE resonant mode centre, which is imperative to ensure efficient Quantum Dot Emitter (QDE) photon capture into ultra-high numerical aperture (UHNA), when operated at cryogenic temperatures. This presentation detailed the multiple steps involved in developing a detailed map from individual tiles to composite mosaic of the whole chip, identifying the QLE structures within matrices and QLE resonant mode centres.

Physics Informed AI for Early Prediction of Solder Joint Degradation in Automotive and Aerospace Power Electronics by Sabuj Mallik, Buckinghamshire New University

High-density electronic assemblies in automotive, aerospace, and renewable-energy systems operate under increasingly severe thermal and vibrational conditions, placing significant demands on solder-interconnect reliability, while conventional qualification methods remain largely reactive and unable to capture early degradation. This presentation introduced a physics-informed artificial intelligence (PI-AI) framework that integrates multi-physics finite-element simulations with machine learning to enable early prediction of solder-joint fatigue. Finite-element analysis was performed on BGA and power-electronics assemblies under combined thermal cycling (–40^{o}C to +150^{o}C) and random vibration loading (up to 14 grms), extracting key degradation indicators including plastic shear strain, inelastic strain-energy density, von Mises stress, and cyclic hysteresis-loop area, alongside realistic mission-profile descriptors. These physics-derived features were used to train a hybrid regression–machine-learning model, benchmarked against experimental fatigue-life data from published studies. The framework achieved over 92% accuracy in predicting crack-initiation cycles, significantly outperforming conventional stress-based approaches, while sensitivity analysis confirmed the dominant role of energy-driven parameters in line with damage-mechanics theory. The approach also produces high-resolution reliability health maps, enabling rapid identification of fatigue hotspots, accelerated design optimisation, improved alloy selection, and enhanced reliability planning for high-density electronic systems operating in harsh environments.

Combining preparation and analysis techniques for studying failure modes within Complex packaging (Power, Chiplet and Multidie) by Lloyd Peto, Nanoscope Services

With increasing package and bonding complexity comes an increase in possible failure modes. This is especially true when different IC's and SMT components are combined into a single package. Modules, Chiplets and complex micro PCB's using a variety of interconnect technologies provide additional challenges for Failure Analysis and Quality Assurance investigations. To support this increase in package complexity a full suite of sample preparation techniques, inspection and elemental analysis techniques are required.

This talk gave examples of the array of capabilities that can be used in combination to provide access to site-specific 3D failures for solving complex packaging problems. Examples of X-ray and CSAM followed by low-stress SMT device extraction followed by Mechanical Sectioning (puck and sandwich) with/without Broad ion Beam polishing, Laser assisted acid decapsulation and device delayering, Silicone removal, Plasma FIB through-die/bump sections, high resolution FIB micro-sections, FIB SI/SE and FEGSEM imaging, EDS mapping of bulk and thin sections and FIBxTEM section extraction from bulk, sectioned, and block biopsy samples – with subsequent (S)TEM imaging and X-ray elemental mapping.

Meet the Sponsors and Exhibitors

Sponsors of MicroTech 2026

Inseto (UK) Ltd - Manufacturing Equipment, Assembly Materials and Adhesives

Exhibitors at MicroTech 2026

Accelonix – Specialist equipment sales and support for Microelectronics, Battery and PCB Assembly

Carl ZEISS - Imaging Solutions for the Semiconductor and Electronics market

Custom Interconnect Ltd – Electronics Manufacturing, Advanced Technologies, Design Services, Power Electronics for BEVs/PHEVs, Box Build and Rapid Prototypes

DISCO HI-TEC Europe – Semiconductor Dicing and Grinding solutions

Eurofins | MASER – Independent service provider for Failure Analysis and Reliability Test

Gen3 - Specialist British Manufacturer and Distributor of Test and Measurement Equipment

INPACK - Advanced IC Packaging, SiP PCB and Oraganic Substrates

IPP Group Ltd - Innovative Inspection, Production and Test Solutions

KLA Corp (SPTS Division) - Advanced Wafer Processing Solutions

Material Consultancy Services (MCS) Group - Applies forensic science to support the design. manufacture, qualification and failure analysis of all kinds of semiconductor. electronic and electro-mechanical systems

SiTEST - Supporting the Semiconductor, Micro-Electronic, Test and Web Inspection Industries

Techworks - is the UK deep tech industry trade association supporting the UK microelectronics industry across the technology spectrum from chip design, manufacturing and packaging to electronic, photonic and software systems and to applications in automotive, power, IoT, cyber security and AI.

Poster Session

The following Posters were presented during the MicroTech 2026 Conference, with an award made for the top poster from Merve University of Glasgow, presented by Suzanne Costello, IMAPS-UK Trustee

MicroTech 2026 Poster Award: Comparative Life Cycle Assessment of Cu-Cu Hybrid Bonding and Copper Micropillar Interconnections for 3D Heterogeneous Integration by Merve Yunlu Dogruyol and Jeff Kettle, University of Glasgow

Electrothermal Modelling of High-Power GaN/SiC Three-level NPC Power Modules by Usha Manasa Ammu[1], Jose Ortiz Gonzalez[1], Tim Rumney[2], Philip Mawby[1] 1 - School of Engineering, University of Warwick, Coventry, UK, 2 - Custom Interconnect Limited, Andover, UK

Functional Re-Use of Recovered Microcontroller Die by Aye Su Mon Kyaw, Joseph Cameron and Jeff Kettle, University of Glasgow

3D Quilt-Packaged ICs on Glass Interposers for Implantable Applications by Chloé Bernardoni[1,2], Ahmad Shah Idil[1,2], Natalia Martinez[1,2], Timothy G Constandinou[1,2] 1 - NGNI Lab, Imperial College London, 2 - Mint Neurotechnologies Ltd, London

Challenges of Solder and Indium Reflow Processes for Detector Chip Hybridisation by Aswathi Koorikkat[1], Han R.[2], Schneider A.[1], Lipp. J. D.[1], Bates R[2]. 1 - UKRI-Science and Technology Facilities Council, Rutherford Appleton Laboratory (STFC-RAL), Harwell Campus, Didcot OX11 0QX, UK, 2 - University of Glasgow, Physics and Astronomy Department, University Avenue, Glasgow G12 8QQ

Heterogeneous Integration – Explained! Workshop – Wednesday 25 March 2026

The Heterogeneous Integration – Explained! Workshop was organised on the afternoon of Wednesday 25 March 2026, at the University of Southampton, which was attended by 57 people.

Heterogenous Integration opens a broad spectrum of packaging solutions that include Flip Chip, Fan Out Wafer Level Packaging, Hybrid Packaging, System in Package, 2.5D/3D and many sub-categories with higher interconnection densities than traditional wire bonding. Challenges include power delivery, signal integrity, multi-physics impacts, IP block interface standards, chiplet manufacturing considerations, warpage and many others. The traditional 2D mindset for device integration in packaging is rapidly changing and a 2.5D and 3D (vertical) integration mindset is becoming a key driver for High Performance Computing, AI, Mobile Products, Power Electronics and Photonics.

This workshop focused on the fundamental aspects of Heterogeneous Integration, explaining the design and assembly requirements, and explored the opportunities for advanced packaging manufacturing solutions in microelectronics, power electronics and photonics. This workshop was complemented with a tour of the facilities at the Southampton Nanofabrication Centre.

For further information on forthcoming events, please visit IMAPS-UK (www.imaps.org.uk)